AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A vector information processing apparatus comprising:

a CPU comprising a plurality of asynchronously operating units;

a main memory for storing data; and

a main memory controller for controlling the writing of data in said main memory, said main memory controller including a vector scatter (VSC) address buffer that holds a storage address in said main memory for each element designated by a vector scatter instruction, wherein said main memory controller inhibits the outputting of a writing permission signal that permits writing to said main memory which is generated according to a writing request that requests writing of an element having a smaller element number than at least one other element designated by the vector scatter instruction if the writing request instructs storage of said element at an identical storage address as said at least one other element and the writing request has not been processed in accordance with a sequence of element numbers defined by the vector scatter instruction,

wherein writing requests for writing said element and said at least one other element to said storage address in said main memory are issued respectively from said asynchronously operating units of said CPU according to said vector scatter instruction.

2. (original): The information processing apparatus according to claim 1, wherein said main memory controller has a plurality of VSC address buffers corresponding respectively to said asynchronously operating units.

3. (original): The information processing apparatus according to claim 2, wherein said asynchronously operating units impart one identifier to a plurality of said writing requests issued according to a single vector scatter instruction, and said main memory controller clears the contents of said VSC address buffers if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

4. (previously presented): The information processing apparatus according to claim 1, wherein said main memory controller comprises:

a VSC address buffer controller for controlling said VSC address buffer to hold said storage address sent from said asynchronously operating units and, if an overflow condition occurs in said VSC address buffer, requests the asynchronously operating unit which has issued a vector scatter instruction that has caused said overflow to resend said element; and

wherein said asynchronously operating unit has a retry buffer for holding each element designated by said vector scatter instruction issued thereby, and resends an element held by said retry buffer to said main memory controller if requested by said main memory controller to resend said element.

5. (original): The information processing apparatus according to claim 4, wherein said asynchronously operating unit corrects the element number of an element which starts to be resent based on a smallest element number, of the elements which start to be resent by each asynchronously operating unit.

6. (original): The information processing apparatus according to claim 4, wherein if said main memory controller detects a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated, said main memory controller sends a delay value for shifting the timing to resend the element from said asynchronously operating unit to said asynchronously operating unit; and

wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller.

7. (original): The information processing apparatus according to claim 5, wherein if said main memory controller detects a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated, said main memory controller sends a delay value for shifting the timing to resend the element from said asynchronously operating unit to said asynchronously operating unit; and

wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller.

8. (original): The information processing apparatus according to claim 4, wherein the number of storage addresses held by said VSC address buffer is set to at least (the number of elements simultaneously processed by said asynchronously operating unit) + 1.

9. (original): The information processing apparatus according to claim 5, wherein the number of storage addresses held by said VSC address buffer is set to at least (the number of elements simultaneously processed by said asynchronously operating unit) + 1.

10. (original): The information processing apparatus according to claim 6, wherein the number of storage addresses held by said VSC address buffer is set to at least (the number of elements simultaneously processed by said asynchronously operating unit) + 1.

11. (previously presented): A method of controlling a memory of a vector information processing apparatus having a CPU comprising a plurality of asynchronously operating units, a main memory for storing data, and a main memory controller for controlling the writing of data in said main memory, said main memory controller includes a vector scatter (VSC) address buffer that holds a storage address in said main memory for each element designated by a vector scatter instruction, said method comprising the step of:

inhibiting the outputting of a writing permission signal that permits writing to said main memory which is generated according to a writing request that requests writing of an element

having a smaller element number than at least one other element designated by the vector scatter instruction if the writing request instructs storage of said element at an identical storage address as said at least one other element and the writing request has not been processed in accordance with a sequence of element numbers defined by the vector scatter instruction,

wherein writing requests for writing said element and said at least one other element to said storage address in said main memory are issued respectively from said asynchronously operating units of said CPU according to said vector scatter instruction.

12. (original): The method of controlling a memory according to claim 11, further comprising the step of:

holding only storage addresses for a plurality of elements designated by a single vector scatter instruction, in said VSC address buffer.

13. (original): The method of controlling a memory according to claim 11, further comprising the steps of:

imparting one identifier to said writing requests issued according to a single vector scatter instruction; and

clearing the content of said VSC address buffer if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

14. (original): The method of controlling a memory according to claim 12, further comprising the steps of:

imparting one identifier to said writing requests issued according to a single vector scatter instruction; and

clearing the content of said VSC address buffer if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

15. (previously presented): The method of controlling a memory according to claim 11, further comprising the steps of:

controlling said VSC address buffer to hold said storage address sent from a plurality of said asynchronously operating units;

if an overflow condition occurs in said VSC address buffer, requesting the asynchronously operating unit which has issued a vector scatter instruction that has caused said overflow to resend said element; and

holding each element designated by said vector scatter instruction in said asynchronously operating unit, and resending an element held by a retry buffer to said main memory controller if requested to resend said element.

16. (original): The method of controlling a memory according to claim 15, further comprising the step of:

correcting the element number of an element which starts to be resent based on a smallest element number, of the elements which start to be resent by each asynchronously operating unit.

17. (original): The method of controlling a memory according to claim 15, further comprising the step of:

if a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated is detected, sending a delay value for shifting the timing to resend the element from said asynchronously operating unit from said main memory controller to said asynchronously operating unit;

wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller.

18. (original): The method of controlling a memory according to claim 16, further comprising the step of:

if a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated is detected, sending a delay value for shifting the timing to resend the element from said asynchronously operating unit from said main memory controller to said asynchronously operating unit;

wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller.

19. (currently amended): The information processing apparatus according to claim 1, wherein writing requests for writing said element and said at least one other element to said storage address in said main memory are issued respectively from different asynchronously operating units of said CPU according to said vector scatter instruction.

20. (previously presented): The method of controlling a memory according to claim 11, wherein writing requests for writing said element and said at least one other element to said storage address in said main memory are issued respectively from different asynchronously operating units of said CPU according to said vector scatter instruction.